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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VANDERPUYE, KENNETH N	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,301	ZAUN ET AL.	
	Examiner	Art Unit	
	Kenneth N Vanderpuye	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-6,10-19 and 38-45* is/are allowed.

6)☒ Claim(s) *2,7-9,20-25,28-33,36 and 37* is/are rejected.

7)☒ Claim(s) *26,27,34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2, 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheung(6,781,601).

With regards to claim 2, Cheung teaches an input processing device(Fig. 3@300) comprising:

an input interface that receives the input data packet(Fig. 3@302, sync); an input processor(Fig. 3@306, parsers) coupled to the input interface to receive input packet data therefrom and write data to a packet buffer(Fig. 3@310); and a packet identifier table coupled to the input processor.(Fig. 3@308, col. 6 lines 55-65), wherein the input processor includes a serial-to-parallel converter for converting the input packet data received from the input interface(col. 6 lines 48-54).

Claim 20 is rejected because Cheung teaches a input processing device, wherein the input processor control logic validates the input packet data by extracting a packet identifier number from a header in the input packet data and checking the packet identifier number with the packet identifier table (control logic is inherently taught because the parsers perform this function, col. 6 lines 55-65).

Claims 21-22 are rejected because Cheung teaches an input processing device, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock field(Fig. 3@328).

Claim 23 is rejected because Cheung teaches an input processor that includes a data delay register that delays the input packet data before the processor writes data to the packet buffer(inherently taught because in order for the parsers to perform a PID comparison, the packets have to be delayed prior to being written to the input buffer).

Claim 24 is rejected because Cheung teaches an input processor that includes a host processor interface.(Fig. 3, bus from sync to the parser).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Gordon et al.(6,481,012).

With regards to claim 7, Cheung teaches an input processing device(Fig. 3@300) comprising:

an input interface that receives the input data packet(Fig. 3@302, sync); an input processor(Fig. 3@306, parsers) coupled to the input interface to receive input packet data therefrom and write data to a packet buffer(Fig. 3@310); and a packet identifier table coupled to the input processor.(Fig. 3@308, col. 6 lines 55-65), Cheung fails to teach wherein the input processor includes a time reference generator that generates timestamp values for the input packets. This is taught by Gordon. (Abstract lines 26-29, Fig. 32). It would have been obvious to one of ordinary skill in the art to combine Gordon with Cheung for the purpose of synchronizing data.

Claim 8 is rejected because Cheung teaches an input processor that includes a host processor interface.(Fig. 3, bus from sync to the parser).

Claims 30-31 are rejected because Cheung teaches an input processing device, wherein the input processor includes a program clock reference detector that checks the input packet data for a valid program clock field(Fig. 3@328).

Claim 32 is rejected because Cheung teaches an input processor that includes a data delay register that delays the input packet data before the processor writes data to the packet buffer(inherently taught because in order for the parsers to perform a PID comparison, the packets have to be delayed prior to being written to the input buffer).

Claim 33 is rejected because Cheung teaches an input processor that includes a host processor interface.(Fig. 3, bus from sync to the parser).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Gordon et al.(6,481,012) and further in view of Allen et al.(5,892,535)

Claim 9 is rejected because both Cheung and Gordon fail to teach an input processing device wherein the processor(parser) is a field programmable gate array. This is taught by Allen(col. 49 lines 53-54). It

would have been obvious to one of ordinary skill in the art to combine Allen with Cheung for the purpose of including a parser, which is user programmable so that users can implement logic designs of their choices.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Gordon et al.(6,481,012)

With regards to claim 36, Cheung fails to teach listing packet identifiers which to be given priority and be processed before non-priority packets. Official notice is taken that the concept of priority filtering it is well known in the art. And is especially used when voice and data packets need to be processed. Voice is delay sensitive than regular data. Hence it would have been obvious to one of ordinary skill in the art to combine this concept with Cheung to the purpose stated above.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Gordon et al.(6,481,012) and further in view of Ryan(5,828,416)

With regard claim 37 Chueng and Gordon fail to teach a processor that discards packets based on using PID. This is taught by Ryan.(col. 5 lines 66-67 to col. 6 lines 1-4). It would have been obvious to one of

ordinary skill in the art discard packets that do no match values on the PID table.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Allen et al.(5,892,535).

Claim 25 is rejected because Cheung fails to teach an input processing device wherein the processor(parser) is a field programmable gate array. This is taught by Allen(col. 49 lines 53-54). It would have been obvious to one of ordinary skill in the art to combine Allen with Cheung for the purpose of including a parser, which is user programmable so that users can implement logic designs of their choices.

Claims 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung.

With regards to claim 28, Cheung fails to teach listing packet identifiers which to be given priority and be processed before non-priority packets. Official notice is taken that the concept of priority filtering it is well known in the art. And is especially used when voice and data packets need to be processed. Voice is delay sensitive than regular data. Hence it would have been obvious to one of ordinary skill in the art to combine this concept with Cheung to the purpose stated above.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung in view of Ryan(5,828,416).

With regard claim 29 Cheung fails to teach a processor that discards packets based on using PID. This is taught by Ryan.(col. 5 lines 66-67 to col. 6 lines 1-4). It would have been obvious to one of ordinary skill in the art discard packets that do no match values on the PID table.

Allowable Subject Matter

Claims 1, 3-6, 10-19, 38-45 are allowed.

Claims 26-27, 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth N Vanderpuye whose telephone number is 7571-272-3078. The examiner can normally be reached on M-F(7:30-5:00) Second Friday Off.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KNV
3/28/05

KENNETH VANDERPUYE
PRIMARY EXAMINER